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Development of High Gain Three Terminal Devices At Millimeter Wave Frequencies

Contract No. N00014-88-C-2088
A Competitive Award
Contract Amount: $570,000

Program Status Report 14-16
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Prepared For

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1. Program Objective

The objectives of this program are: to develop high gain three terminal devices at millimeter wave frequencies. Specifically, InGaAs pseudomorphic high electron mobility transistors (HEMT) will be developed in four key areas: materials, device models, processing, and characterization. The 36 month program consists of two tasks. Task I is to develop the high gain transistor with 6 dB gain, 0.3 W/mm power density, and 20% efficiency at 60 GHz in the first 12 months. Task II is to develop transistor with at least 6 dB of gain , 0.25 W/mm power density and 15% efficiency at 94 GHz and to assess the reliability of the transistor in the next 24 months.

2. Progress

Progresses were made in device processing with new DH InGaAs pseudomorphic (PM) wafers grown by Columbia University. The layer structures were discussed in a previous monthly report and is given again in Fig. 1. Wafers #2-242 and 2-243 contain a double heterojunction (DH) structure which has two charge supplying layers. The In% of the InGaAs pseudomorphic channel layer is 20% and the Al% of the AlGaAs layers is 25%. Wafer #2-243 is identical to Wafer #2-242 except that a GaAs spacer layer was added below the pseudomorphic InGaAs channel to improve the interface quality. These two wafers were processed to E-Beam lithography gate device level using the new High Gain Transistor mask set. One wafer already completed DC and on-wafer S-parameter tests.

The testing results showed DC transconductances of 480 mS/mm to 580 mS/mm, and cutoff frequencies f_t of 80 to 90 GHz for both 80 and 100 μm gate width devices and 68 to 75 GHz for 50 μm gate width devices. This wafer has exhibited a comparable DC performance but better RF S-parameter performance than that of the previous wafers, such as 3838-1, which gave the best V-band power efficiency and density so far. Fig. 2 showed the SEM of a InGaAs pseudomorphic HEMT on this wafer with 0.15 μm gate length (The SEM has a magnification of 30,000 times) and its DC characteristics, Gm and

Ids vs Vgs. The device has a peak Gm of 480 mS/mm at a gate voltage of 0.6 V and with 232 mA/mm current density. The maximum current density of the device reaches about 390 mS/mm.

As part of the device development, we studied the back gating effect for the DH InGaAs pseudomorphic HEMT devices. Fig 3 contains a device layout showing a back gate contact placed next to the drain. The back gate contact provides the electrical connection to the buffer layer. The transconductance and the drain current of the device seemed to depend on the backgate voltage. Fig. 3 shows Gm and Ids as a function of gate voltage under two backgate bias conditions: +10 V and -10 V. The transfer curve for the device under +10 V backgate bias differentiate itself with a marker. The device under +10 V backgate bias exhibits some serious sub-threshold conduction, possibly due to the traps in the bottom n-AlGaAs layer. Basing on previous results of DH InGaAs pseudomorphic HEMTs, we have found that the effect is most noticeable when Al composition in the AlGaAs layer is greater than 20% and when the silicon doping density in AlGaAs is greater than 2 $X10^{18}$ $1/cm^3$. Having n-AlGaAs layers with 25% Al and doped to 4 x 10^{18} $1/cm^3$, this wafer fits to the description of the one which would have sub-threshold conduction. However, the sub-threshold current was eliminated when the device was biased with a backgate voltage of -10 V, because the charges in the AlGaAs traps were depleted. Using the backgate voltage we could investigate the material quality of the buffer layer and its impact on device performance as demonstrated here. We can also conclude that the material quality of the bottom AlGaAs charge supply layer has a greater impact on the device performance than the one above the InGaAs channel.

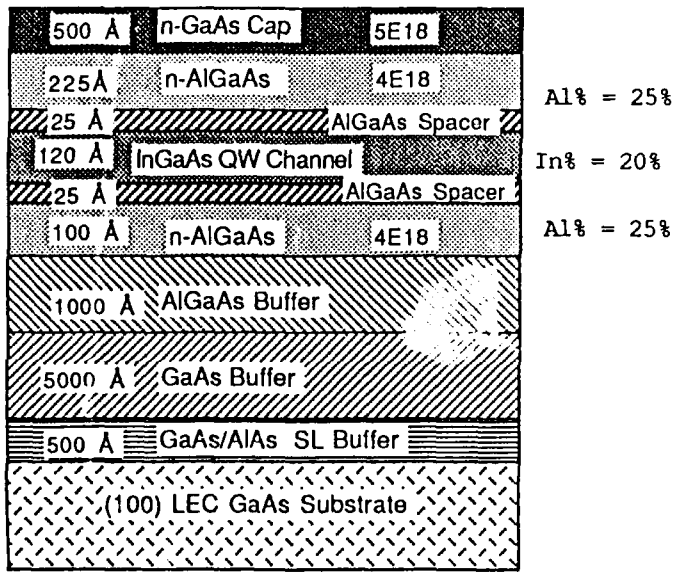
3. Plan

We will grow some DH InGaAs HEMT epi wafers with a newly installed Varian Gen II D system at TRW for this program. We will also continue device processing for existing wafers.

InGaAs Pseudomorphic HEMT

DH HEMT Epi structures (Wafer #2-242, #2-243)

InGaAs/AlGaAs Pseudomorphic
DH HEMT
(Wafer # 2-242)



InGaAs/AlGaAs Pseudomorphic
DH HEMT with Added GaAs Spacer
(Wafer #2-243)

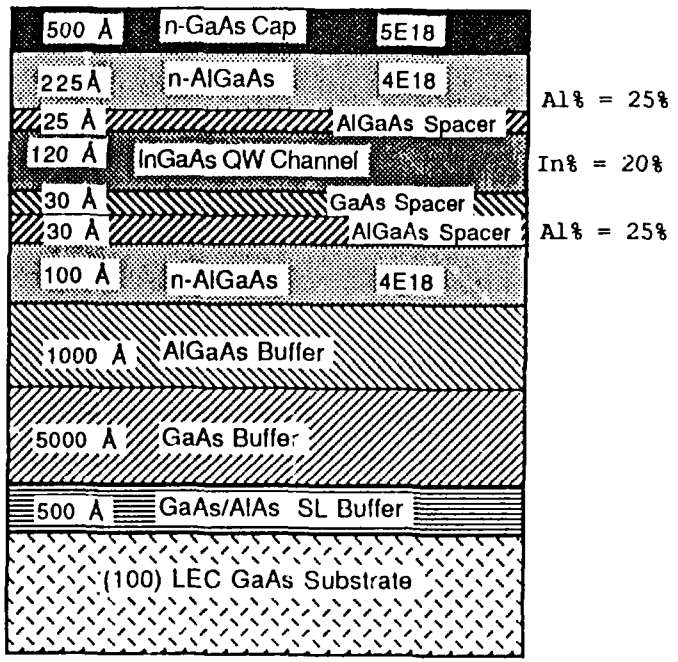
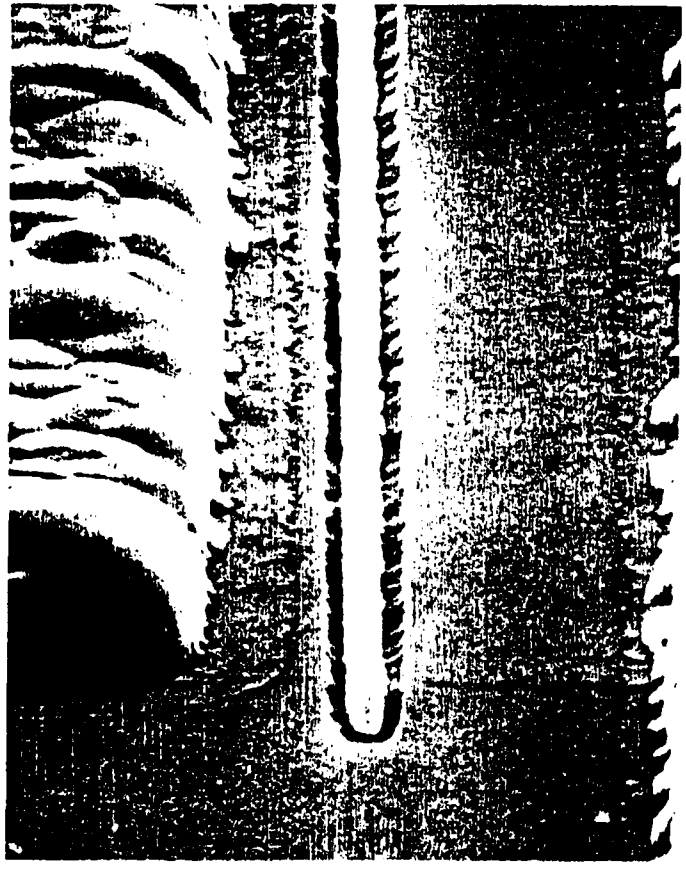


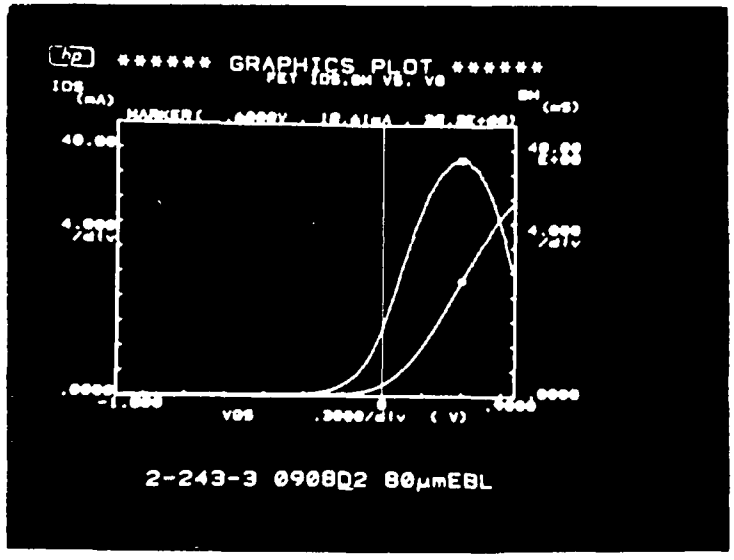
Fig. 1

InGaAs Pseudomorphic HEMT

Device SEM and DC characteristics



Gate Length = 0.15 μm

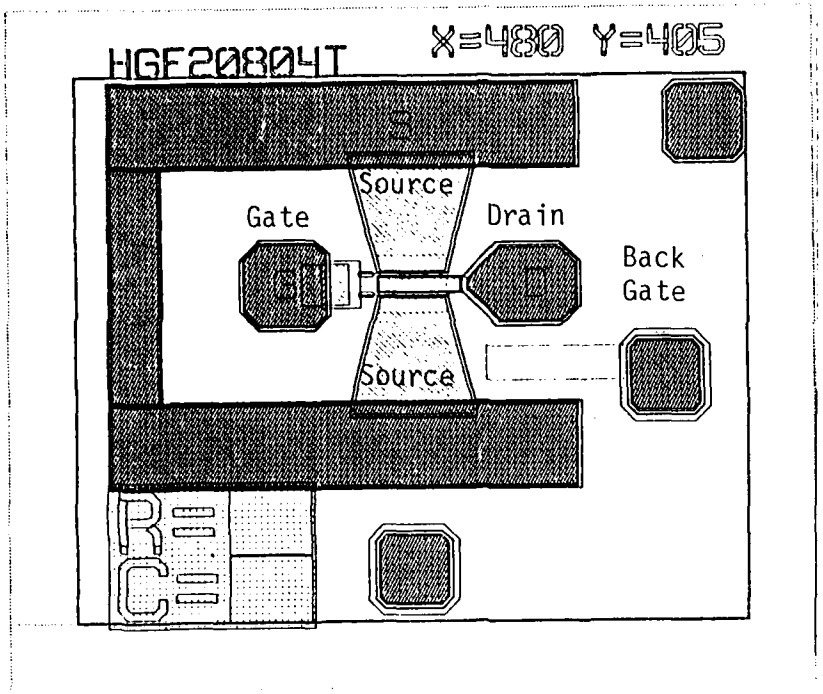


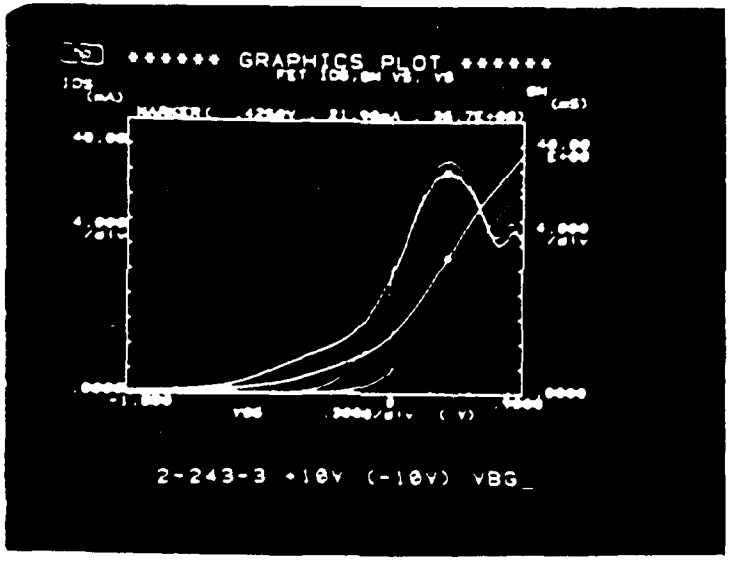
Gmp = 480 mS/mm

Fig. 2

InGaAs Pseudomorphic HEMT

Back Gate Contact and DC characteristics





Back Gate Voltage = +10 V and -10V

Fig. 3

Development of High Gain Three Terminal Devices At Millimeter Wave Frequencies

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1. Program Objective

The objectives of this program are: to develop high gain three terminal devices at millimeter wave frequencies. Specifically, InGaAs pseudomorphic high electron mobility transistors (HEMT) will be developed in four key areas: materials, device models, processing, and characterization. The 36 month program consists of two tasks. Task I is to develop the high gain transistor with 6 dB gain, 0.3 W/mm power density, and 20% efficiency at 60 GHz in the first 12 months. Task II is to develop transistor with at least 6 dB of gain , 0.25 W/mm power density and 15% efficiency at 94 GHz and to assess the reliability of the transistor in the next 24 months.

2. Progress

During this program month, we completed device processing of two quarter wafers (3838-2 and 3795-2). These two quarters were from the same wafers which had shown good DC/RF performance (3838-1 and 3795-1). Typically, we process two-inch HEMT wafers up to optical-gate test device level and then quarter the wafer for subsequent E-beam lithography process. The reason for dividing HEMT wafers into quarters for E-beam gate process is to provide more trying opportunities for wet-chemical gate etching, which is still the most critical step in HEMT processing. Present high performance InGaAs pseudomorphic (PM) HEMT process often requires gate recess etching to a depth 200 Å above the conducting two-dimensional electron gas channel. It is unlikely that a tight gate recess control like this and an optimal recess depth could be obtained in one try. The quarters of a wafer enhance the chance of successful gate recess depth to achieve the best performance.

As we had reported previously, both 3838-1 and 3795-1 wafers showed good DC device performance and 3838-1 wafer gave the best V-band RF performance in terms of power added efficiency, power density, and gain. We also found in RF testing that the current capability of HEMT device is essential in achieving high power density and high efficiency. We therefore

processed the two new quarters from 3838 and 3795 to achieve higher current capability than the previous quarters. The InGaAs PM HEMTs of 3838-2 wafer with a gate length of 0.15 μm exhibited a drain current density of over 440 mA/mm and with a typical transconductance of 400 to 500 mS/mm. In comparison, the devices on the previous 3838-1 wafer were capable of only half the current density at the same transconductances. Fig. 1 shows a device SEM and DC characteristics of a HEMT on 3838-2. The SEM showed another importance feature which is the wide gate recess undercut. The wide undercut could inprove device breakdown voltage and efficiency. However, only after RF power testing to be conducted later for the device could we confirm such a claim.

Devices of 3795-2 wafer (DH-Double Heterojunction HEMT) also had a higher current capability (620 mA/mm with Gmp about 400 to 480 mS/mm) than that of 3795-1 wafer, which only exhibited 360 mA/mm current density at the same Gmp. The SEM and DC characteristics of a device on 3795-2 are shown in Fig. 2.

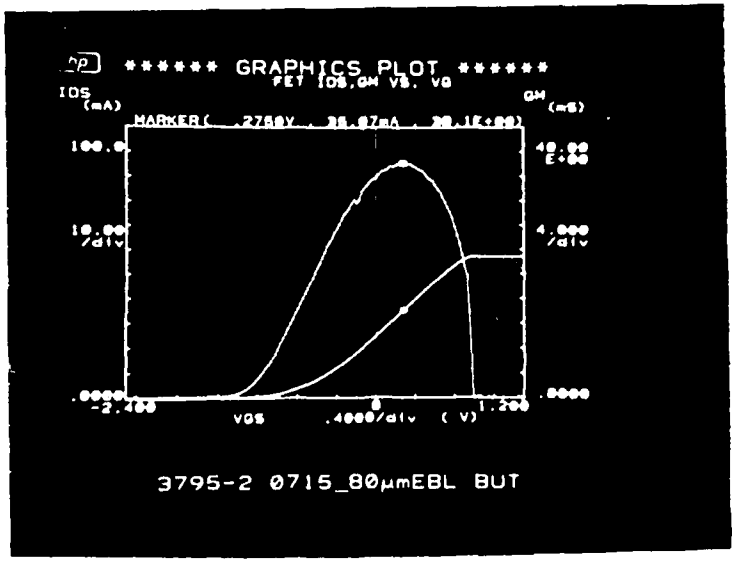
3. Plan

We will continue the backside process for wafers 3838-2, 3795-2, and 2-243-3 and RF test the devices when the wafers are scribed. We will grow InGaAs PM HEMT materials with TRW's newly installed Varian Gen II D system.

InGaAs Pseudomorphic HEMT (DH)

Device SEM and DC characteristics

(Wafer 3795-2)



Ids = 620 mA/mm for Gmp = 400 mS/mm

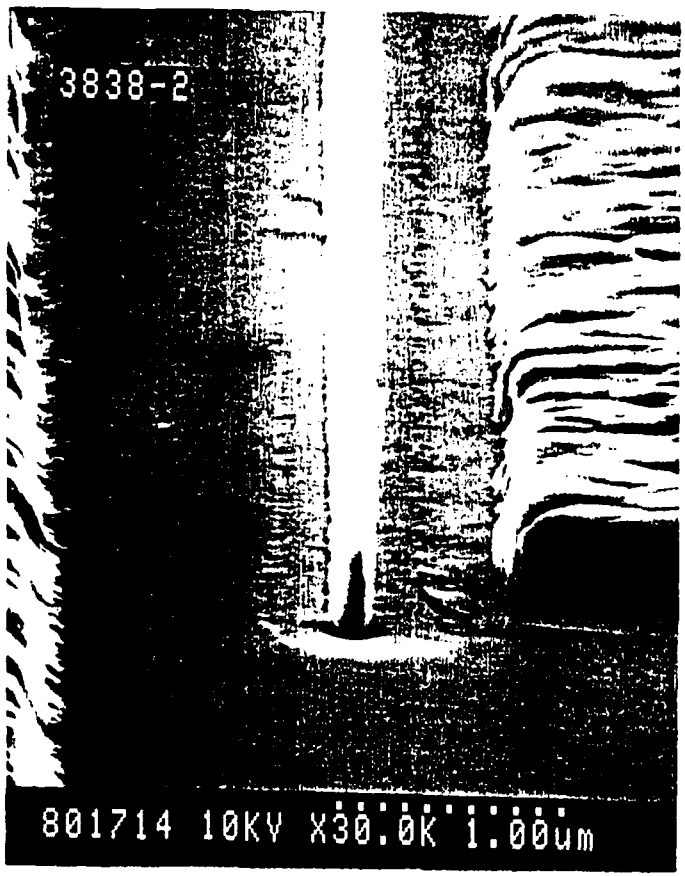
Gate Length = 0.15 μm

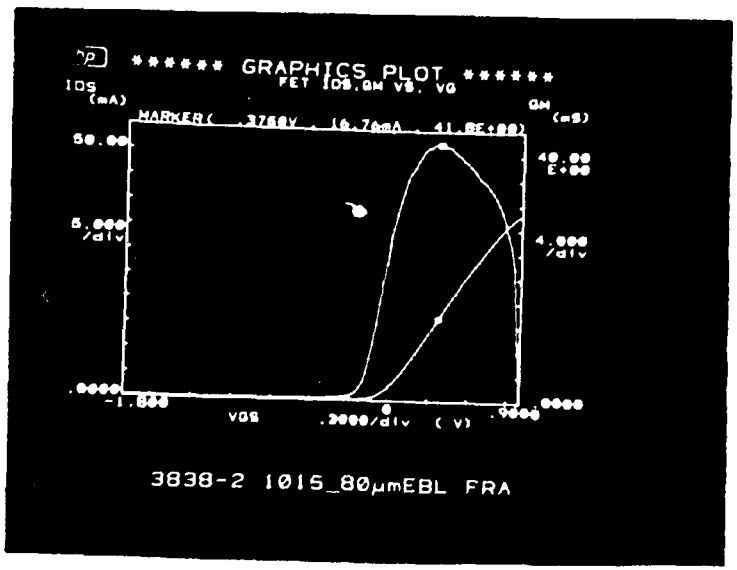
Gmp = 476 mS/mm

Figure 1

InGaAs Pseudomorphic HEMT

Device SEM and DC characteristics (Wafer 3838-2)





Gate Length = 0.15 μm

Ids = 440 mA/mm for Gmp = 400 mS/mm

Gmp = 523 mS/mm

Figure 2

Development of High Gain Three Terminal Devices At Millimeter Wave Frequencies

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2. Progress

During this month, we completed backside process and scribing for three quarter wafers 3838-2, 3795-2 and 2-243-3. The two quarters, 3838-2 and 3795-2 were from the same wafers which had previously shown good DC/RF performance. We processed these two new quarters to achieve higher current capability than the previous quarters. The InGaAs pseudomorphic (PM) HEMTs of 3838-2 wafer with a gate length of 0.15 μm exhibited a drain current density of over 440 mA/mm and with a typical transconductance of 400 to 500 mS/mm. In comparison, the devices on the previous 3838-1 wafer were capable of only half the current density at the same transconductances. Devices of 3795-2 wafer (DH-Double Heterojunction HEMT) also had a higher current capability (620 mA/mm with Gmp about 400 to 480 mS/mm) than that of 3795-1 wafer, which only exhibited 360 mA/mm current density at the same Gmp. Wafer 2-243-3 was a Columbia University grown MBE wafer with a DH epi structure and processed with the new mask set "High Gain HEMT". It was scribed to chips for MIC amplifier fabrication and RF characterization. Wafer 3795-1 was an old wafer processed to final chips a few month ago and is ready for RF characterization. These four wafers all together will be packaged onto a MIC low noise amplifier housing for RF characterization at 60 GHz. The V-band housing with a mounted HEMT device is shown in Fig. 1 along with a penny coin to show the size of the V-band amplifier housing.

During the program month, we have completed MBE growth for 7 wafers, which comprised the two new wafer lots, lot 5 and lot 6. So far 19 MBE wafers were grown for this program, and the detailed structure of each wafer in terms of its epitaxial layers are given in Fig. 2. We have processed all MBE wafers to various stages in fabrication and most of them will be processed to completion. At least a quarter from all wafers of lot 1 to lot 4 completed EBL process so far and was DC and RF characterized. Good DC and RF performance was demonstrated from devices of these wafers. Among them, 4 quarters are waiting to be evaluated at V-band with InGaAs pseudomorphic HEMT devices from the wafers packaged in MIC amplifiers. Wafers from lot 1 through lot 3 were grown with a TRW Gen II system, the first Gen II system at TRW. Wafers from lot 5 and lot 6 were grown with a newly installed MBE machine at TRW, the Gen II D modular MBE system. Wafers from lot 4 were grown by Columbia University. Single heterojunction (SH) InGaAs PM HEMTs and double heterojunction (DH) HEMTs were the main device structures for this program. The doped channel approach was tried in lot 3 only. The new mask set was used for wafers from lot 3 and later lots. Details of device structures of the wafers grown in this program thus far are shown in Fig. 2. The main device structure features are the cap layer, AlGaAs charge supplier layer, spacer, InGaAs channel, bottom spacer and charge supply layer for DH structures, and buffers. Our device optimization efforts included the epi-layer design, device processing and DC and RF testing with results feedback to device design.

3. Plan

We will characterize the MIC LNAs fabricated with the four wafers-3795-1, 3795-2, 3838-2, and 2-243-3. We will continue device processing for the newly grown wafers. A few new InGaAs pseudomorphic HEMT wafers will be grown, among which a MBE wafer will be delivered to NRL, while 5 transistors and a processed wafer were already selected and waiting for delivery.

InGaAs Pseudomorphic HEMT
V-Band Amplifier Housing

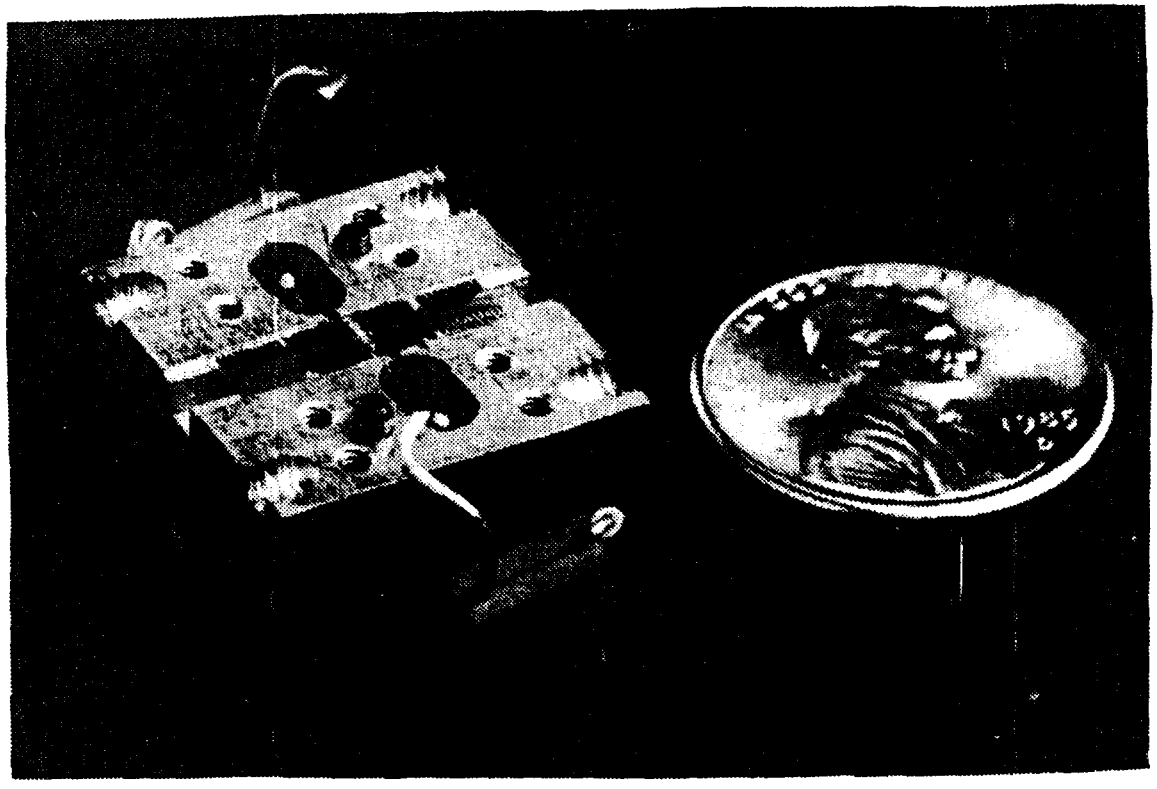

Figure 1

InGaAs Pseudomorphic HEMT
MBE wafers and structures

Lot	Wafer	Epi Type	Mask Used	Cap n-GaAs thickness/doping (Å, 1/cm3)	AlGaAs (Å)	n- AlGaAs thickness/doping (Å, 1/cm3)	Al %	AlGaAs spacer (Å)	InGaAs channel (Å)	In %	Buffer	DH spacer (Å)	DH supplier thickness/doping (Å, 1/cm3)
1	3788	DH	LNF2	400, 4E18	200	250, 4E18	15	50	190	15	AlGaAs	30	125, 2E18
1	3795	DH	LNF2	400, 4E18	200	250, 4E18	15	50	190	15	AlGaAs	30	125, 2E18
1	3838	SH	LNF2	400, 4E18		250, 3E18	15	50	190	15	SL* + GaAs		
2	3933	DH	LNF2	400, 4E18	200	250, 4E18	15	50	130	15	AlGaAs	30	250, 4E18
2	3934	DH	LNF2	400, 4E18	200	250, 4E18	15	50	130	15	AlGaAs	30	200, 4E18
2	3935	DH	LNF2	400, 4E18	200	250, 2.5E18	15	50	130	15	AlGaAs	30	250, 4E18
3	3958	DCDH	LNF2	400, 5E18	G150	100, 3.8E18	15	(2E18DC)	190	15	AlGaAs		250, 4E18
3	3959	DCDH	LNF2	400, 5E18	G150	100, 3.8E18	15	(5E18DC)	50+120	15	AlGaAs	30	250, 4E18
3	3985	DCDH	HG	400, 5E18	G150	100, 3.8E18	15	(2E18DC)	130	22	AlGaAs		250, 4E18
3	3986	DCDH	HG	400, 5E18	G150	100, 3.8E18	15	(5E18DC)	70+80	22	AlGaAs	30	250, 4E18
4	2-242	DH	HG	500, 5E18		225, 4E18	25	25	120	20	AlGaAs	25	100, 4E18
4	2-243	DH	HG	500, 5E18		225, 4E18	25	25	120	20	GaAs+AlGaAs	30+30	100, 4E18
5	D1042	DH	HG	500, 6E18	300	Si PD 5E12	28	30	150	20	GaAs+SL	10	50, 6E18
5	D1044	DH	HG	400, 6.4E18	200	Si PD 4E12	28	20	150	20	AlGaAs	15	70, 4.3E18
5	D1045	DH	HG	400, 6.4E18	200	Si PD 4E12	28	20	190	15	AlGaAs	15	70, 4.3E18
5	D1046	DH	HG	400, 6.4E18	200	Si PD 4E12	28	20	190	15	GaAs+AlGaAs	10	50, 6.4E18
6	D1047	SH	HG	400, 7E18	200	125, 5E18	28	20	190	15	GaAs+SL		
6	D1062	SH	HG	300, 7E18	300	Si PD 4.5E12	28	20	150	20	GaAs+SL		
6	D1063	SH	HG	300, 7E18	300	Si PD 5E12	28	20	175	20	GaAs+SL		

Figure 2